Notice of Allowability	Application No.	Applicant(s)	
	09/996,865	PAK ET AL.	
	Examiner	Art Unit	
	Chuong D. Ngo	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers filed on 09/23/2005*.

2. ☒ The allowed claim(s) is/are *3 and 7-11*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Chuong D Ngo
Primary Examiner
Art Unit: 2193

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with applicant's representative, David C. Ashby on 10-07-2005.

The application has been amended as follows:

Claim 3 has been replaced by:

- - 3. A dynamic adder comprising:
a plurality of dynamic domino circuits arranged into a plurality of stages, wherein each of said plurality of dynamic domino comprising:
a logic portion adapted for processing logic of said dynamic domino circuit,
a first dynamic output portion coupled to said logic portion, said first dynamic output portion having a first dynamic node for dynamically holding a first data,
a second dynamic output portion coupled to said logic portion, said second dynamic output portion having a second dynamic node for dynamically holding a second data,
a third dynamic output portion coupled to said logic portion, said third dynamic output portion having a third dynamic node for dynamically holding a third data,
a first and a second transistors having their gates coupled to said first dynamic node, said first transistor having its drain coupled to said second dynamic node, said second transistor having its drain coupled to said third dynamic node,
a third and a fourth transistors having their gates coupled to said second dynamic node, said third transistor having its drain coupled to said first dynamic node, said fourth transistor having its drain coupled to said third dynamic node, and
a fifth and a sixth transistors having their gates coupled to said third dynamic node said fifth transistor having its drain coupled to said first dynamic node, said sixth transistor having its drain coupled to said second dynamic node;
and
a multiplexer coupled to a final stage comprising:

a latch built into said multiplexer, and

a first and a second dynamic select inputs to said multiplexer, wherein said multiplexer functions as a latch using said latch when said first and said second dynamic select inputs are precharged to logic zero, and wherein said multiplexer functions as a multiplexer when said first and said second select inputs are evaluated to their respective logic values. - -

Claim 7 has been replaced by:

- - 7. A dynamic adder to generate dynamic logic inversions comprising:

a plurality of dynamic domino circuits arranged into a plurality of stages, wherein at least one stage comprising a dynamic circuit implementing a mutually exclusive circuit to compute groups of three terms carry logic, wherein the value of each of the three terms carry logic is represented as a dynamic output computed as a function of true terms;

wherein the mutually exclusive circuit includes three dynamic output portions representing one for each of the three terms carry logic where each dynamic output portion is coupled to gates of transistors whose drains are coupled to the other dynamic output portions such that the output of a selected dynamic output portion is exclusive of the values of the other dynamic output portions, and wherein groups of said three terms carry logic comprises group propagate (gp), group generate (gg), and group kill (gk), and

a multiplexer coupled to a final stage comprising:

a latch built into said multiplexer, and

a first and a second dynamic select inputs to said multiplexer, wherein said multiplexer functions as a latch using said latch when said first and said second dynamic select inputs are precharged to logic zero, and wherein said multiplexer functions as a multiplexer when said first and said second select inputs are evaluated to their respective logic values. - -

3. The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or fairly suggest a dynamic adder as recited in the claims that includes a multiplexer coupled to a final stage of the adder wherein the multiplexer functions as a latch when a first and second dynamic select inputs are precharged to logic zero, and functions as a multiplexer when the first and said second select inputs are evaluated to their respective logic values as recited in claims 3 and 7.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong D Ngo
Primary Examiner
Art Unit 2193

10/07/20057